

41st STUDENT CONFERENCE (E2)
Student Team Competition (3)

Author: Mr. Nishchay Mhatre
College of Engineering Pune, India, mhatrens07.it@coep.ac.in

Mr. Mohit Karve
College of Engineering Pune, India, mkarve@ncsu.edu
Mr. Gautam Akiwate
College of Engineering Pune, India, gautam.akiwate@gmail.com
Mr. Shravan Aras
College of Engineering Pune, India, arassg08.comp@coep.ac.in
Mr. Sanjeev Krishnan
University of Pune, India, sanjeevmk4890@gmail.com
Mr. Varad Deshmukh
College of Engineering Pune, India, varad.deshmukh@gmail.com
Mr. Rahul Bedarkar
University of Pune, India, falconer.nsm@gmail.com

A MODULAR, GENERIC, LOW-COST ON-BOARD COMPUTER SYSTEM FOR NANO OR PICO
SATELLITE APPLICATIONS**Abstract**

The need for a generic, extensible On Board Computer (OBC) system for small satellite missions, which can be developed at a low cost in a developing nation, is felt. Advances in technology, dropping costs of embedded system components and the availability of Free and Open Source development tools for both hardware and software have the potential of giving an impetus to such development. Such a system has been developed and described in this work. The purpose of the system is to serve as a robust computing and control platform for a variety of small satellite missions with various payloads. Its current role is as the OBC of the CCOMSAT (COEP Communication Satellite), which has a Ham communication payload. A modular design approach has been followed. The system can be tailored effectively to different mission profiles by re-arranging, modifying or upgrading modules. This also facilitates updating the system with improving technology. The project is also meant to serve as the training ground in this design methodology, for students. The fundamental and generic problems of computing and controlling in space were studied, namely power constraints, 'real-time' requirements, fault tolerance, space environment hazards and system integration along with the peculiar constraints of nano/pico satellite systems. The modules - processing element, storage, communication interfaces, fault tolerance and recovery, single-event upset protection, inter-subsystem and intra-subsystem interfaces, were identified. Then the independent modules were developed by small teams and then tested and integrated. Innovative solutions for problems like RTOS implementation, single event upsets, HILS, were found. Extensive black-box and clear-box tests were conducted on the software while the hardware was similarly bench-tested. A Hardware In the Loop System (HILS) is under construction for testing the system with respect to the interactions with other subsystems in the satellite. The detailed design and implementation of the modules is described. The results of the tests reflect the readiness of the modules to be integrated and used in the engineering model of the satellite and are summarised in this work. We also describe how the particular modules utilise cutting edge technology available to us and the procedures developed for testing and integration

of the modules and modification according to mission specific requirements. Finally, the development of the design process is explored, with respect to advantages and disadvantages, lessons learnt and useful caveats.