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COMPACT AND HIGH PERFORMANCES EQUIPMENT FOR VISION-BASED NAVIGATION

Abstract

The paper is dedicated to the presentation of the RD activities carried out by TSD, in the framework of the MOSS project, co-financed by the Italian Space Agency, for the design and development of compact and high performances equipment for vision-based navigation. Vision-based navigation can be considered as a major enabling technology in support of the autonomy requirements of space applications like: Exploration missions (landers, rovers, etc.) On-Orbit Servicing Applications (like Satellite Inspections, Rendezvous, Docking etc.) Formation-Flying Missions The MOSS project is aimed at developing the following equipment: Multi-ocular Camera CMOS Monocular Camera CCD Monocular Camera integrated with motorized lens High-performance Processing Unit for Visual Navigation (HPVN)

The Multi-ocular camera is a three sensors camera supporting: 3D stereo vision with two 1Mpixel monochrome sensors Panoramic vision based on one color HD image sensor

The CMOS Camera is a single sensor 1080p high resolution color camera.; its compactness (69.5x69.5x51mm), low mass (310grams), low power consumption (2.2 to 3.5W), and the embedded compressor makes possible to employ it also on board very small space platform like Nanosatellite. The CCD Camera is equipped with a HD CCD color sensor and it is integrated with motorized lens offering autoiris, autofocus and zoom. All the cameras are provided with a redundant CAN bus I/F for configuration control purposes, and with a LVDS SerDes link I/F for uncompressed video transmission to the HPVN or other processing units; two mono-ocular cameras are furthermore provided with a SpaceWire I/F that can be used to output compressed video directly to the spacecraft OBDH. The HPVN is dedicated to image processing. It comprises a fault tolerant single board computer based on a complex System-On-Chip designed around the Leon3FT CPU soft IP core implemented in Actel antifuse radiation tolerant Axcelerator FPGA. A mezzanine card supports LVDS SerDes camera interface and implements hardware accelerated image processing algorithms in high-density radiation tolerant space-grade Xilinx Virtex-5QV FPGA. Main on-board resources are duplicated and can be configured in parallel to implement a single point failure architecture or in a master-slave mode, so to run in parallel to improve processing capabilities. The unit can support up to 4 HD video inputs, loss-less and/or lossy compression, feature detection and tracking, real-time disparity map calculation. All the above described parts are available in two radiation tolerance levels.