SPACE SYSTEMS SYMPOSIUM (D1)
Enabling Technologies for Space Systems (2)

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THE NEXT GENERATION OF SPACEFLIGHT PROCESSORS: LOW POWER, HIGH PERFORMANCE, WITH INTEGRATED SPACEWIRE ROUTER AND PROTOCOL ENGINES

Abstract

There is a continuous demand for more and more processing power on-board spacecraft to handle sophisticated instrument control, mathematically intense data processing and compression, and real-time attitude and orbit control. In addition, increasing autonomy of spaceflight systems requires intelligent on-board management of spacecraft resources. The required processing capability has to be provided at minimal power consumption and it has to be readily integrated into the on-board data-handling and avionics systems. The Atmel AT6981 is a new radiation-hard-by-design processor being developed by Atmel to fulfill this need, providing exceptional processing power per mW and integrating a comprehensive set of peripheral interfaces.

At the heart of the AT6981 is a SPARC V8 processor with on-chip instruction and data caches and an integrated IEEE754 floating-point unit. 1 Mbyte of fast static random access memory (SRAM) is provided on-chip, enough to support many instrument control and processing applications. Where additional memory is required a memory management unit and external memory interface makes adding external SRAM and DDR memory devices straightforward. The on-chip peripheral interfaces include SpaceWire, MIL-STD 1553, CAN, SPI, UART and Ethernet.

The AT6981 is designed with extensive integrated support for SpaceWire applications using STAR-Dundee SpaceWire technology. It includes an embedded SpaceWire router with eight external ports and internal ports for connecting to three SpaceWire protocol-handling engines. The SpaceWire Engines offload SpaceWire protocol handling from the SPARC V8 processor each supporting the Remote Memory Access Protocol (RMAP) Initiator and RMAP Target protocols. The RMAP Initiator handles the sending of RMAP commands and the receiving of RMAP replies. The processor can set up a series of commands in memory and inform the RMAP Initiator, which then takes over, sending the RMAP commands and receiving the replies, placing any received data in memory. The RMAP Target provides support for external devices to read and write directly to memory informing the processor once data transfer has completed. The SpaceWire Engines also handle other SpaceWire protocols through a protocol selective DMA controller, providing support for emerging SpaceWire plug and play and other, future, protocols. The SpaceWire links each operate at up to 200 Mbits/s.

The AT6981 includes a Debug Support Unit with debugging over UART or SpaceWire interfaces. A comprehensive software development toolset is available including debug support.

The full paper will provide full details of the AT6981 processor. It will explain how this processor can be used to fulfill many spacecraft on-board processing requirements.