SYMPOSIUM ON BUILDING BLOCKS FOR FUTURE SPACE EXPLORATION AND DEVELOPMENT (D3)
Systems and Infrastructures to Implement Future Building Blocks in Space Exploration and Development (2)

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RECONFIGURABLE DUAL-CORE SYSTEM-ON-A-CHIP FOR SPACE AVIONICS

Abstract

Future space avionics requires high reliability, high performance and low power consumption. With high-performance commercial processor cores and radiation-hardened-by-design (RHBD) standard cells, it is feasible to create space-grade system-on-a-chips (SoC's) on advanced nano-meter CMOS technology. However, commercial cores targeting consumer electronics lack architectural properties for single-event-effect (SEE) detection, isolation and recovery as server-class processors. Dual cores in a lock-step fashion are often used to archive 100% SEE detection at the expense of doubling power consumption. Since applications have different reliability requirements, we propose a new hardware-software approach to compensate additional power consumption by unlocking the two cores and providing a normal dual-core SoC. The reconfigurable dual-core SoC is implemented with standard processor cores, which has only on-chip-bus interfaces, interrupts and no other special ports. So it is possible to apply the architecture described in this article to any processor cores. Architectural simulation, fault analysis and fault injection experiments are performed and the results show this architecture provides both high reliability and high performance.