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Educational Pico and Nano Satellites (4)

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AN INTEGRATED, COMPACT AND ROBUST RF DESIGN FOR A PICOSATELLITE COMMUNICATION SYSTEM

Abstract

Designing and testing the communication system for a cubesatellite imposes inherent challenges and restrictions. Picosatellites having form factors like 1-U and 2-U, have limited power and space available for incorporating a reliable, powerful and robust communication system. The half-duplex Communication system for 'Swayam', a 1-U cubesatellite has been designed for low Earth orbit HAM communication. The radio frequency (RF) system design plays particularly important role in these satellites to ensure the overall efficiency of the system. Factors affecting system performance include component placement, circuit design and impedance matching techniques. Module wise impedance matching networks implemented for the Communication system involves the use of L-C components forming an L-section using lumped elements. The circuit performance was thoroughly evaluated and the performance compared with hand calculations to estimate the effects of factors like component placement, discrete component self-resonant frequency, device S-parameters, Quality factor and printed circuit board (PCB) routing techniques. Through an iterative approach the optimum matching elements and the arrangements of various layers on the PCB

were derived for the best RF performance. For improving system reliability and robustness, a provision has been incorporated to switch to a bypass link in case of contingencies on the high power amplifier or the low noise amplifier, thus directly connecting the transponder to the duplexer. The algorithm implemented on the Terminal Node Controller (TNC) effectively switches between the available links for the communication interface. Factors like temperature that affect the system's stability and cause drifts in transponder frequency have been compensated through the communication protocol software. A novel feature adopted for testing and evaluating the system parameters includes modularization of the RF blocks and making provisions for RF test points, without compromising the circuit performance and the overall form factor 83.8 mm x 79.27 mm. This paper pertains to the lessons learnt during the design and evaluation of the RF system, covering the overall architecture of the system, impedance matching methodology as well as the hardware iterations and performance validation for the same.