EARTH OBSERVATION SYMPOSIUM (B1)
Earth Observation Data Management Systems (4)

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LOSSY MULTI/HYPERSPECTRAL COMPRESSION HW IMPLEMENTATION AT HIGH DATA RATE

Abstract

Image compression is becoming more and more important, as new multispectral and hyperspectral instruments are going to generate very high data rates due to the increased spatial and spectral resolutions. Transmitting all the acquired data to the ground segment is becoming a serious bottleneck, and compression techniques are a feasible solution to this problem. The CCSDS has established a working group (WG) on Multispectral and Hyperspectral Data Compression (MHDC), which has the purpose of standardizing compression techniques to be used onboard. The WG has already standardized a lossless compression algorithm for multispectral and hyperspectral images, and has started working on a lossy compression algorithm. The complexity of lossless compression algorithms is typically larger than that of lossless ones, leading to potentially lower throughputs. Therefore, a careful assessment is required in order to identify techniques that are able to sustain very high data rates. The increased complexity can also lead to increased resource occupancy on a hardware device such as an FPGA. Lossy compression introduces information losses in the images, and these losses must be accurately characterized, and their effect on the applications investigated. For these reasons, developing a lossy algorithm requires a more elaborate process. It is required that the compression algorithm, when implemented in HW, shall be capable of sustaining a real time data throughput in the order of 20 Msamples/s, with a pixel depth up to 16 bits per sample. Under an ESA contract primed by Politecnico of Torino, TSD is currently designing an IP core for FPGA and/or ASIC implementation of a lossy compression algorithm that is being proposed for CCSDS standardization. In addition to the IP core, TSD is developing a HW platform based on the Xilinx Virtex-5XQR5VFX130, the industry's first high performance rad-hard reconfigurable FPGA for processing-intensive space systems. Advanced results along with details of electronic platform design will be presented in this paper.