SPACE SYSTEMS SYMPOSIUM (D1)
Poster Session (P)

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EVALUATION OF MEMORY RELIABILITY IN A DUAL MICROCONTROLLERS ON-BOARD COMPUTER ARCHITECTURE

Abstract

The outer space can greatly affect the reliability of programmable electronic systems and it is considered as one of the most difficult environment for embedded systems due to harsh conditions. In space, high-energy particles and frequent temperature variations are the main reasons of Single event upsets. While the use of commercial off-the-shelf components and scaled transistors, opposed to radiation-hardened elements, increases the memory capacity, it increases also the susceptibility to the external factors mentionned above. Radiations and temperature variations can modify the physical properties of transistors (e.g. Static Noise Margin) in memory devices and lead to a temporary corruption of data or even to a permanent destruction of the internal cell structure. This paper presents an innovative On-Board Computer (OBC) architecture for small stellites and the results of a campaign of fault-injection test realized in the laboratory of the Institut Supérieur des Sciences et Techniques (INSSET) of Saint-Quentin, France. The OBC architecture is based on the implementation of two software processing units with different characteristics and functionalities. The Main Unit (MU) used to realize the mission has very high performances and a large capacity of memory but is not radiation-hardened. The Controller Unit (CU), although completely reliable and able to whistand the harsh space environment has low performances if compared to the Main Unit. The two units give to the system the ability to perform various embedded diagnostic tests and it has been developed especially a technique to measure the level of reliability for each memory cell in the MU. The technique is based on the interpretation of statistical data obtained after a write and read test cycle perform by the CU. The fault injection test campaign that will be pesented in the paper is based on a custom-built fault injection test bench using a JTAG probe. The injection of memory faults has been carried out according to specific models and in a completely random way. This architecture will be implemented on the OBC of the IP2 Sat CubeSat, planned to be launched next years and also as a secondary payload of one satellite of the QB50 project.