66th International Astronautical Congress 2015

SPACE SYSTEMS SYMPOSIUM (D1)
Interactive Presentations (IP)

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A RELIABLE MULTICORE PROCESSOR DESIGN FOR SPACE APPLICATIONS

Abstract

Currently, the trend in commercial processor of stepping forward to many cores on a single die has posed an opportunity and a challenge for China's space mission. The opportunity is to use multiple core to increase performance for current diverse space processing application while limiting power dissipation to extend the life time of the payload for the mission. The challenge is to guraantee the reliability in a harsh environment. This paper will discuss the reliable multicore processor developed for the space application and explore the capability to satisfy the extremely tight power and budget constraints in space missions. The discussion is about:(1). Analyzing the schemes to achieve fault-tolerance in a multicore processor; (2). Describing the architecture of our own many-core processor, codenamed Revealer16; (3). Characterizing some special features involved in the Revealer16 processor and the tradeoff adapted for the practical space applications; (4). Experimental exploration using the Revealer16 processor for reliable computing. Based on the Revealer16, we implemented several widely used kernels, such as matrix multiplication, vector addition/multiplication, FIR filter and 2D-FFT, which all support 32 bits integer, 32 bits single-precision float and 40 bits high-precision float operations. We measured and analyzed the performance of these kernels. The Revealer16 processor based on a 2D-meshed NoC network shows potential high-performance and low-power dissipation at a low error rate to current space based processors.