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REVEALER1601-RH : A RADIATION HARDENED NOC-BASED MULTICORE DIGITAL SIGNAL PROCESSOR

Abstract

Future space exploration poses an orders of magnitude performance requisite conundrum beyond current onboard computing ability. As always have been proven, commercial multicore processor enables revolutionary performance improvement than typical uniprocessor, thus giving an opportunity to leverage this tendency in space applications. Since the reliability is not the priority concern for commercial off the shelves (COTS) devices, the usage of COTS multicore processors poses a challenge for designer to use such devices in extremely challenging environments to defect the single event effects (SEES). In this paper, we propose the design requirements of a real NoC (Network-on-Chip) based 16-core processor for reliable space computing and the approaches to deliver such capability with schedule, cost, power and weight and volume constrains. Starting with a discussion of faults and errors in microprocessor and multicore processor, we first briefly introduce the gross and comprehensive faults detection and error recovery mechanisms in multicore processor. Then the architecture of a COTS multicore processor – Revealer1601 is presented and used as a prototype for the further development of a reliable aero-specific high performance computing (ASHPC). In light of the above mentioned detection and recovery mechanisms, we explore the gross hardening techniques which can be applied with the consideration of minimal overhead. Here, we give the key design points of the radiation hardened (RH) vision – Revealer1601-RH processor, making it a real practical verification in space design.

In this paper, we only take account to the hardware reliable techniques employed in the design. Salient techniques include: memoried hardening with EDAC (Error Detection and Checking); microarchitecture redundancy with SIMD processing lanes; massive on-chip register monitoring by automatic netlist insertion; fault-tolerant NoC communication and fault-tolerance in high speed data exchange interface.

The Revealer1601-RH processor based on a 16-core Revealer1601 architecture illuminates the ASHPC aspects in many applicable areas. The chip is fabricated on a commercial CMOS process in 65nm technology with the hardening on library cells. The die area is 15065μm×15063.5μm with 16W power consumption. Each core can run 400MHz after Place&Route with GALS clocking. The chip will be packaged with

ceramic BGA packaging. The heavy ions injection test and total ionizing dose (TID) test are carrying out and the soft error rate is expected to be less than $1e-5 Error/Device\dot{D}ay$. At the end, we discuss the potential application areas of the Revealer1601-RH processor and summarize how a low cost methodology can be applied to harden a commercial tile-meshed multicore.