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DUPLICATED VOTING PROCESSORS FOR THE LOW COST RADIATION HARDENING OF COMPUTERS

Abstract

The problems caused by radiation induced errors in satellite computers can have mission critical effects. Due to the extremely high cost of radiation hardened processors, small and innovative space missions must often accept the risks of computers not protected against radiation. Furthermore, the rapid improvements in processor capabilities are rarely reflected in radiation hardened processors due to the lengthy development cycles and low demand.

With the computer architecture tested in this research an alternative to radiation hardened processors appears to be possible. Through the utilization of 3 identical processors and respective peripherals, referred to as nodes, a comparison strategy allows for the rapid detection and mitigation of radiation induced errors. The three nodes utilize a software based comparison of each-others processes to detect bit flips that may have affected calculations. The nodes also compare each others current consumption. If an erroneous node is detected the other two nodes perform a vote of non-confidence, triggering the only radiation hardened component, a NAND array. Once the NAND array is triggered by two votes of non-confidence, the erroneous node has its power supply switched off, allowing any stray radiation induced charge to drain before the node is rebooted. With this computer architecture it is theoretically possible to utilize most modern processors and create a radiation hardened computer, without the high costs normally associated with such endeavors.

This computer architecture has been tested on systems utilizing Atmel ATmega2560 processors and systems utilizing STMicroelectronics STM32F4 processors. Both these processors were chosen for their simplicity of prototyping and relatively low power consumption, allowing for the required triplicate implementation without consuming an excess of power. In testing this method of radiation protection has proven effective against simulated latch up and bit flip events in a node. Most notably it allows for the effective removal of the threat of a latch-up induced permanent system failure, with no system downtime needed to recover, as well as the removal of bit flip induced corruption of critical calculations and variables in the processors.

Testing using proton beam radiation is planned for later in 2017 to confirm the test results. A main on board computer utilizing this architecture with STM32F4 processors is planning to be launched as part of the UBC Orbit Thunderbird 0 CubeSat mission in late 2018 or early 2019.