SMALL SATELLITE MISSIONS SYMPOSIUM (B4) Space Systems and Architectures Featuring Cross-Platform Compatibility (7)

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THE DESIGN AND IMPLEMENTATION OF RECONFIGURABLE COMMAND AND DATA HANDLING SUBSYSTEM FOR SCIENCE TECHNOLOGY SATELLITE-3

Abstract

This paper describes the design and implementation of Command and Data handling Subsystem(CDS) for an advanced small satellite 'STSAT-3 (Science and Technology SATellite-3)' of Republic of Korea. CDS of STSAT-3 is composed of On-Board Computer(OBC), Mass Memory Unit(MMU) and TeleCommand TeleMetry Unit(TCTM). OBC manages the spacecraft and payload according to the schedule set by G/S and provides environment for AOCS Flight Software, MMU stores payloads data and sends them to the G/S via X-band channel and TCTM apply bi-level commands and samples the analog and digital sensors. CDS of STSAT-3 is on-orbit reconfigurable subsystem which is based on Leon3 Fault Tolerant Processor by uploading FPGA code and S/W code. By which we can modify, upgrade and even change the system during mission. For reliable system Triple Module Redundancy(TMR) technology and configuration memory scrubbing algorithm is applied to protect FPGA and Error Detection and Correction algorithm(EDAC) is applied to protect memories in space application. Many functions are implemented in FPGA such as Reed-Solomon code, loseless compression code and Protocol Processing code of STSAT-3 for high speed data processing. Function test and space environment test was successfully performed and it satisfies the requirements of STSAT-3.