Paper ID: 4265
student

SMALL SATELLITE MISSIONS SYMPOSIUM (B4)
Design and Technology for Small Satellites - Part 1 (6A)

Author: Dr. Toshinori Kuwahara
University of Stuttgart, Germany

Mr. Marek Dittmar
University of Stuttgart, Germany
Prof. Hans-Peter Roeser
University of Stuttgart, Germany
Mr. Claas Ziemke
Private, Germany

FPGA-BASED ON-BOARD COMPUTERS FOR RECONFIGURABLE COMPUTING ON SPACE SYSTEMS

Abstract

The goal of this paper is to present the development status of the Field programmable gate array (FPGA) based On-board computer for Reconfigurable computing on Space systems (FORS), which is currently under development at the Institute of Space Systems of the Universitaet Stuttgart. FORS is designed for Low Earth Orbit applications and especially optimized for small satellites. It is internally organized in a combination of multiple SRAM-FPGAs and Flash-FPGAs. In order to mitigate radiation effects, Single Event Upsets (SEUs) in the multiple redundant SRAM-FPGAs are monitored, detected, isolated and recovered from the monitoring Flash-FPGA, which is inherently immune against SEUs. The relatively high vulnerability of Flash-FPGAs is the bottleneck of the system reliability, which is estimated as 0.89 in 2 years. For the Flash-FPGAs, the newest product line of Actel, RTA3P is selected, while the SRAM-FPGAs are based on Xilinx COTS Virtex devices. Currently, engineering model is under development and the breadboard model of the system is already available and its functionality is under verification.

Compared with traditional microprocessors, the merits of applying FPGA technologies is the possible speed-up factors of up to almost four orders of magnitude, as well as reduction in electricity consumption by more than one order of magnitude, although the clock frequency remains substantially lower than that of microprocessors, which are very attractive to small satellite applications. Furthermore, direct implementation of hardware interfaces into the FPGA chips is optimal for the realization of a highly integrated central computing unit for small satellites. The unification of different computing functions aboard the satellite onto a single computer system results in clear-cut system structure and provides a high degree of fault tolerance with minimal resources. The first flight model of FORS is designed for the central computing unit of the first small satellite within the Stuttgart Small Satellite Program and demonstrates its high computational capability performing operations of camera instruments (up to 25 m GSD), accurate attitude control (7 arcseconds pointing knowledge), and telecommunication (up to 500Mbit/s).