Paper ID: 43479
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IAF MATERIALS AND STRUCTURES SYMPOSIUM (C2)
Specialised Technologies, Including Nanotechnology (8)

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A NEWLY DEVELOPED RADIATION HARDENED NOC-MESHING MULTICORE DIGITAL SIGNAL PROCESSOR FOR HIGH AEROSPACE COMPUTING PERFORMANCE

Abstract

In this paper, we propose the definition, architecture and implementation of a real Noc (Network-on-Chip)meshing processor with heterogeneous integration to meet space computing requisites. The approaches to deliver extremely computing capability with schedule, cost, power and weight and volume constrains are reviewed.

Future space exploration poses an orders of magnitude performance requisite conundrum beyond current on-board computing ability. As always has been proven that commercial multicore processor enables revolutionary performance improvement than typical uni-processor, opportunities are posed to leverage this tendency in space applications to use multicore for perfomance demanding. Coupled with these appealing opportunities are the challenges of reliability as the priority concerns when deploying such devices in extremely harsh environments to defect the single event effects (SEE).

Along this strategy, we start this text with a discussion of faults and errors in microprocessor and multicore processor. We first briefly introduce the gross and comprehensive faults detection and error recovery mechanisms in multicore processor. Then the architecture of a COTS (Commercial Off the Shelves) multicore procesor, Revealer1601, is presented and used as a prototype for the ftuuther development of a reliable aero-specific high performance computing platform. In light of the above mentioned error detection and recovery requirements, we explore the hardening techniques which can be applied with the consideration of minimal overhead. Here, we give the key design points of the radiation hardened (RH) vision, Revealer1601-RH processor, making it a real practice in space deploying.

With emphases on hardware hardening, techniques employed in Revealer1601-RH design are discussed in this paper, including memories hardening with EDAC (Error Detection and Checking), micro-architecture redundancy with SIMD processing lanes, massive on chip register monitornng by automatic netlist insertion, fault-tolerant NoC communication and fault-tolerance in high speed data exchange interface.

The Revealer1601-RH processor has been fabricated on a commercial CMOS process in 65mm technology with the hardening on library cells. The die area is 15065μm $\times$15063.5μm with 16W power consumption. Each core can nun 400MHz after PlaceRoute with GALS clocking strategy. The chip is packaged with ceramic BGA packaging. The heavy ions injection test and total ionizing dose(TID) test are carying out and the soft eror rate is expected to be less than $1e-5Erro/Device-Day$. At the end,

we discuss the potential application areas of the Revealer1601-RH processor and summarize how a low cost methodology can be applied to harden a commercial tile-meshed multicore.