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DESIGN OF FAULT TOLERANT SYSTEM FOR THE ON-BOARD COMPUTER OF STUDSAT-2

Abstract

STUDent SATellite (STUDSAT-2) is India's first twin-Nano satellite project being developed by students under the guidance of Indian Space Research Organization (ISRO). The project aims to demonstrate in-orbit separation, inter-satellite communication and drag-sail mechanism.

One of the bottlenecks of Nano satellites is its mission life. The shorter mission life may be due to one of the two reasons. Firstly, the constraints on the volume of the satellite limits the scope of energy capacity which in turn degrades the survivability of the satellite. Also, the adverse and hostile environments in space necessitate the need for space-grade components in the design which is unavailable to students. The paper presents a design mechanism that could ensure the improved mission life despite the problems presented above.

On-Board Computer (OBC) plays a vital role in functioning of the satellite. Even a slight malfunction of OBC would result in failure of entire mission. Malfunction of OBC may be either due to hardware or software flaws. The paper presents a method to recover the system stability under both cases.

We propose a fault tolerant system by introducing a single level redundancy to the OBC of the system. The primary system is under periodic monitoring for its readiness. A Back-up system is kept in warm standby and takes control once it detects the failure of the primary. Failure through software errors could be a Flash corruption. This crisis can be tackled by storing the image of flash in an external non-volatile memory. Periodically flash memory of the system is checked for corruption and will be re-programmed with the image stored in external memory if found faulty.

Although the proposed method enhances the mission lifetime, it adds to the overall mass, power, cost and volume of the system. Nevertheless, the reliability of the mission being the primary goal of a satellite, the proposed system is feasible.

Currently the system is being implemented with a single level redundancy wherein the primary is being monitored for every 54s (10% of the duty cycle). The implemented system is working reasonably well under the failures either due to hardware or software.