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IMPROVED THROUGHPUT SATELLITE SYSTEM USING EFFICIENT TRANSCEIVER ARCHITECTURE

Abstract

Satellite communication systems are one of the most growing fields due to the increasing demand for satellite services and applications. In addition to the conventional satellite applications such as video/audio broadcasting and communications, satellite systems are currently used for many other applications such as remote sensing, earth observation, positioning, navigation systems, and weather forecasting. Such applications are precious for the humanity and it has been integrated into various civil and military services.

Although satellite systems do not suffer from the spectrum scarcity problem, which is a major challenge for other wireless systems, the need for improving satellite systems throughput is a pressing matter. For example, in low earth orbit satellites (LEO), the connection between the satellite and earth station is in the order of minutes where the satellite has to download a massive amount of data in the form of images or videos. Therefore, increasing the throughput will have a high impact on the system efficiency. Moreover, improving the throughput will reduce the energy cost per information bit, which is very beneficial for satellite systems due to their limited power resources. Using efficient error control coding and higher order modulation schemes is currently one of the key technologies to increase the throughput of various communication systems. Particularly, with the introduction of advanced error control coding schemes such as turbo product codes (TPC) and low density parity check codes (LDPC).

The aim of this paper is to develop, evaluate and implement advanced algorithms that can be integrated into high throughput satellite systems. The targeted algorithms that will be explored include advanced modulation schemes and capacity-approaching error control techniques. Moreover, the developed system will utilize low complexity algorithms to minimize the computational complexity, which directly contributes to improving the processing power and hardware lifetime.