

IAF SPACE EXPLORATION SYMPOSIUM (A3)
Interactive Presentations - IAF SPACE EXPLORATION SYMPOSIUM (IP)

Author: Mr. Carlos Posse
Spin.Works S.A., Portugal, carlos.posse@spinworks.pt

Mr. Francisco Câmara
Spin.Works S.A., Portugal, francisco.camara@spinworks.pt

Mr. João Oliveira
Spin.Works S.A., Portugal, joao.oliveira@spinworks.pt

Mr. José Canilho
Spin.Works S.A., Portugal, jose.canilho@spinworks.pt

Mr. Tiago Hormigo
Spin.Works, Portugal, tiago.hormigo@spinworks.pt

IMPLEMENTATION AND FLIGHT TESTING OF CPU+FPGA VISUAL BASED NAVIGATION AND
HAZARD DETECTION AND AVOIDANCE FOR PLANETARY LANDING**Abstract**

This work presents the results of an effort to implement visual based navigation (VBN) and hazard detection and avoidance (HDA) algorithms to run in real-time in space-grade hardware platforms for future planetary and small body missions. Existing software-only algorithms went through a significant re-design effort to explore the parallelism and deep pipe-line processing offered by CPU+FPGA architectures, speeding up the VBN and HDA algorithms. HDA algorithms were ported to a LEON2 processor and a co-processor FPGA built on a Microsemi ProASIC A3PE3000 FPGA, compatible with the RTAX2000 series of space qualified fuse-link FPGA. For the VBN algorithm, the Zynq-7020 SoC was selected as the hardware development platform. The processing hardware set was then programmed with the CPU+FPGA-optimized algorithms, connected to a processor-in-the-loop high-fidelity descent and landing simulation tool, and an extensive performance assessment campaign followed. To prepare for flight testing, a transportable Avionics Test Bench (ATB) was built, capable of carrying the processing hardware running the VBN algorithms and the payload management system, the VBNHDA Sensors suite composed of COTS sensors including an IMU, visual camera, imaging LIDAR, and laser range finder, and additional electronic components like mass memory, communication telemetry and power distribution board. The Zynq-7020 co-processing FPGA was programmed to handle both the required on-board sensor interfaces and the processing IP blocks that compose the VBN hardware accelerators. The performance results presented in this work are based on actual testing with the ATB. The discussion focuses on the comparison between CPU-only and CPU+FPGA approaches to VBN and HDA algorithms. Performance is measured in terms of processing speed, algorithm performance degradation and impact on the navigation accuracy. Processor-in-the-loop (PIL) Monte Carlo results show a safe landing probability of 99.42% (1193/1200 cases), yielding a 91.20% confidence level that unsafe landing is <1% likely. The 7 remaining cases are attributable to GNC error: the selected landing site is safe in these cases, but the GNC is not precise enough to avoid all other nearby hazards. The PIL scenario is a powered Mars descent and landing, where HDA takes <10s and the VBN runs at 10Hz, using images of 512x512 and 100-150 tracked features. Cumulative horizontal error between image acquisition and landing is then <4m (3- σ), with a final landing dispersion of 6.5m (3- σ sigma equivalent).