SMALL SATELLITE MISSIONS SYMPOSIUM (B4)
Design and Technology for Nano-Sats and Cube-Sats (6B)

Author: Mr. Lucas Antunes Tambara
Southern Regional Space Research Center - CRS/CCR/INPE - MCT in collaboration with the Space Science Laboratory of Santa Maria - LACESM/CT - UFSM, Brazil

Dr. Nelson Jorge Schuch
Southern Regional Space Research Center - CRS/CCR/INPE - MCT in collaboration with the Space Science Laboratory of Santa Maria - LACESM/CT - UFSM, Brazil
Dr. Adriano Petry
Southern Regional Space Research Center - CRS/CCR/INPE - MCT in collaboration with the Space Science Laboratory of Santa Maria - LACESM/CT - UFSM, Brazil
Dr. Andrea Schwertner Charão
Universidade Federal de Santa Maria - UFSM, Brazil
Mr. William do Nascimento Guareschi
Universidade Federal doRio Grande do Sul - UFRGS, Brazil

ALTERNATIVES TO REDUCE THE POWER CONSUMPTION IN FPGA IMPLEMENTATIONS APPLIED IN NANOSATELLITES

Abstract

Nanosatellites require efficient designs because of their restrictions on mass, volume and surface area implying on the power supply reduction. Their power subsystems are designed specifically for the simplicity and efficiency. Therefore, some restrictions must be considered in order to use Field Programmable Gate Array (FPGA) in a nanosatellite. This is because the power consumption can become high on these devices compared to an Application-Specific Integrated Circuit (ASIC) device, since the signal path are generally longer. Therefore, it is essential to try to reduce the power consumption in circuits based on FPGA. The alternatives to reduce the dynamic power consumption are analyzed, which means that the dissipated power should be considered for the loading and unloading of the logic gates. The architectures and methods studied were: static analysis, reduction of glitches, pipelined architecture, dynamic management of the clock signal and clock gating. All these methods try to reduce the number of changes in signal level. Among them, preliminary analysis shows that the most efficient is the pipelined architecture. It can achieve a reduction in consumption of up to 58% in some devices. Another benefit of the pipelined architecture is that usually it also implies the reduction of glitches.