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A NOVEL ACQUISITION ARCHITECTURE FOR GNSS RECEIVER BASED ON DOWN SAMPLING AND CORDIC ALGORITHM

Abstract

Acquisition is one of the key function modules of the baseband system of satellite navigation receiver to perform a correlation with the satellite baseband signal and local PRN code. As the parallel code phase search based on FFT can acquire not only the code phase shift but also the Doppler frequency shift of the carrier signal at the same time, it has been widely used in GNSS receiver. However, some defects appear in the application of the parallel code phase search algorithm. As the length of FFT is related to the sample frequency, and the length of sampled data always can't be expressed by the 2's integer power, so the realization of FFT processor can't complete the FFT operation such as this length. Under this situation, a conventional method is adding 0 by the following of the sampled data. The shortcoming of this method is that we must increase the length of the FFT processor, it will lead to more hardware consumption and higher power, especially for the hand-hold receiver, reducing the hardware consumption and depressing the power is very critical. In a GNSS navigation receiver for GPS, GLONASS and COMPASS, in order to acquire the three navigation signals at different chip rates, three different FFT processors are needed when using the parallel code phase search algorithm, it further increases the consumption of the hardware. In response of this situation, a novel acquisition architecture is proposed. This architecture is based on the down sampling rate averaging technique and CORDIC algorithm. In this architecture, the sampled data are converted into 1024 through a down sampling module, which can reduce the length of the FFT effectively, and the twiddle multiplications are performed by CORDIC-based multipliers, it avoids the hardware multiplier which always occupies a lot of hardware resource. Besides, because of the feature of CORDIC algorithm, the architecture can save the memory resource effectively. The experiment results show that the proposed acquisition architecture can greatly reduce the power and hardware consumption while keeping the fast acquisition. The hardware resource and the memory resource in the proposed architecture are 62.5% and 50% respectively compared with the conventional algorithm, which may be attractive for the GNSS navigation receivers.