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HARDENING AGAINST RADIATION OF SOFTWARE CODE IN COTS PROCESSORS FOR LOW-COST NANOSATELLITES

Abstract

The protection against radiation of the software code present in every commercial COTS processor-based sub-system within low-cost nanosatellites is a mandatory task in its design. This paper presents a general methodology depicting how to address the overall protection of this code to mitigate software errors. The code is supposed to be written in either C/C++ or assembly language. COTS devices running this code are supposed to suffer from all possible Single Event Effects (SEE): single event upsets (SEU), both single (SBU) and multiple (MBU), single event functional interrupts (SEFI) and possibly others. They are also supposed to: survive a certain desired total ionization dose (TID) presented in its operational environment (a given orbit with given operational lifetime) and be either latchup-free or protected from disruptive radiation-induced effects by appropriate external devices.

The hardening strategy takes into account different levels of abstraction, when applying the proposed techniques: hardening of data-driven and control-driven routines, program flow, interrupts service routines, data storage and system (re)configuration. This situation induces different implementation techniques and different resources utilization to achieve a better protection. In this way, this paper proposes the use of "smart watchdogs", low-level code modifications (assembly code) and high-level language additions/modifications when necessary within the running scenario.

The design of this methodology has been made using UML (Unified Modelling Language) and does a heavy use of its benefices. In this way the problem is modelled using classes, use cases and sequence diagrams. The hierarchical design of the hardening methodology has led us to a better understand of the problem.

With respect to commonly used techniques, the proposed approach allows using commercial C compilers with commercial off-the-shelf CPUs (e.g. Texas Instruments' MSP430 family of processors) and produces a code which is optimized in size with respect to other automatic approaches to SW hardening. This improvement is due to the higher level at which the task of SW hardening is analyzed, which allows system-level and mission-level optimizations.

The strategy has been tested on the Texas Instrument's commercial MSP430 family and extensively used to develop the modular architecture ARAMIS for low-cost satellites.