SPACE SYSTEMS SYMPOSIUM (D1)
Enabling Technologies for Space Systems (2)

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# SYSTEM-ON-CHIP DESIGN FOR DATA HANDLING ON-BOARD SMALL SATELLITES

**Abstract**

There is a growing trend towards small and intelligent spacecraft. More and more researchers are looking into sub-kilogram satellites, e.g. picosatellites, for future space missions. For example, the CubeSat platform has been widely accepted by universities over the world for education and research purposes. Most CubeSats to date are less than 1kg, for which the launch cost can be affordable for universities. However, from the previous launches of the CubeSats it shows that single CubeSat has limited applications for space missions. This is because the limited resources on-board in terms of area, power and computing capability. On average, solar panels for CubeSats provide no more than 2.4W power per panel hence why most developers choose low-power and low-frequency micro-controllers for data handling on-board satellites. The volume of a CubeSat is 10cm x 10cm x 10cm, which cannot accommodate most scientific instruments for missions.

At the Surrey Space Centre a novel approach is proposed to use picosatellites for future space missions. The 'Satellite Sensor Network' applies the concept of terrestrial wireless sensor networks to networked spacecraft. The satellite sensor network can be applied to many practical space missions: 1. it is capable of virtual satellite missions, which emulate a large spacecraft; 2. it can take on tasks of remote monitoring, diagnostics and self-repair, ensuring correct operation, longer life and higher quality of service; 3. it could be used as co-orbiting assistants/inspectors of larger mother ships; 4. it could provide continuous Earth coverage for monitoring or communication at low cost; and finally it can be deployed around the Moon, Mars and other planets or asteroids to provide continuous communications for multiple low-powered surface vehicles.

To carry out these missions the on-board computers are required to execute computation-intensive tasks, for example formation-flying control to keep a 'safe' distance between satellites and avoid collisions; optimised signal routing within the network; high-performance computing for on-board signal processing and etc. The current off-shelf embedded processors are hard to meet our requirements in terms of power and speed. Instead a system-on-chip approach is adopted at the Surrey Space Centre. The system-on-chip design is centric on the AMBA bus, with all the IP cores being connected to this bus. The main processing unit is a LEON3 CPU, running at more than 100MHz, which switches on/off the peripheral IP cores for power efficiency. Targeting these satellite sensor network missions, many new peripheral IP cores are developed. The medium access controller for inter-satellite link is capable for signal routing and task scheduling within the network. The image compression core greatly reduces the load for sending images while consumes very low power. The Java optimised processor runs Agents for satellite network management in real-time. A SRAM-based FPGA is used to implement the system-on-chip. Partial run-time reconfiguration is developed to mitigate radiation effect for space applications.