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SYSTEMC-BASED SPARC V8 MMU RESEARCH AND DESIGN

Abstract

Now many companies and research institutes favor SPARC microprocessors for their high reliability in embedded domain, for example, industrial controls, military electronics and space applications. Furthermore, SPARC V8 has been used widely on astronautical products of many countries. With the complexities of processing tasks, embedded processors need operating systems for multitasking and communication. So the processors call for Memory Management Units (MMUs), then they can translate virtual addresses into physical addresses and provide memory protection among multiple contexts. In addition, in order to reduce cost, researchers always simulate hardware platforms to evaluate performance before production. In this paper, we develop a simulation system based on SystemC. It simulates a SPARC V8 processor's MMU, including contexts switching, page-level matching, segment-level matching, region-level matching, context-level matching, multiple virtual addresses mapping the same physical address, whole TLB (Translation Lookaside Buffer) or single TLB flushing, TLB miss processing, switching between user mode and supervisor mode and so on. The experiments prove that the system is convenient and reliable.