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# SMALL FOOTPRINT FAULT TOLERANT 8/16-BIT PROCESSOR FOR SPACE APPLICATIONS

**Abstract**

In many onboard data handling applications like on board sensors, actuators, communication nodes and other compact payloads the implication of available 32-bit fault tolerant (FT) processors present excessiveness in terms of performance, power consumption and design complexity. On other hand, there usually are many more suitable counterparts mostly originating from Components-Off-The-Shelf (COTS) that have existing flight heritage information and even in some cases the radiation profile has been obtained. However, whilst COTS are at least in part unavoidable for affordable aerospace applications, as the next generation space technologies, products and eventually complete missions forward today's trends of lowering the costs, the lack of integrated Single Event (SE) effects mitigation techniques and other common Fault Detection, Isolation and Recovery (FDIR) approaches typically imposes additional supervisory hardware and software structures to achieve adequate level of performance under given radiation profile. The main motivation for the work presented by this paper was to introduce fault tolerance at the level of a compact, configurable, scalable and highly flexible 8/16-bit processor core for on System-On-Chip (SoC) design approach to provide reasonable ratio between performance and design complexity with consequential costs and power requirements, whilst ensuring high availability and data integrity for distributed applications. Incorporation of FDIR policy at the earliest stages of the design is provided by a flexible and comprehensive fault mitigation scheme. The paper presents a newly designed and developed fault tolerant processor core called PicoSky, which is based on Harvard enhanced RISC pipelined architecture, providing a rich and powerful instruction set with high code density to lower the memory requirements. Integrated FT features provide operation in user and supervisor mode with several error detection trap handlers. Seamless switching between operational modes assures that traps are handled completely independent from the current state of user application. The processor architecture provides several protection mechanisms to prevent erroneous operations from single event transient (SET) and single event upset (SEU) errors. The core is based on triple modular redundancy (TMR) using a word voter approach rather than bit wide voting schemes used in conventional TMR systems. Beside this, additional skew can be programmed to improve SET effects prevention on account of maximum achievable performance. Finally, results are provided in terms of core performance and resource usage for Field Programmable Gate Array (FPGA) implementations as eventually the focus is to achieve a small footprint for a single chip embedded system solutions using cost effective Flash based FPGAs.