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HARDNESS ASSURANCE EVALUATION OF MICROCONTROLLERS FOR SATELLITE ELECTRONICS WITH LASER PULSES

Abstract

Some phenomena in the physical environment of microcircuits such as, high-energy charged particles, gamma radiation, stray electric fields and random Electro-Magnetic Interference (EMI) cause single event faults in electronic devices. In this situation, the logical state of digital components changes by depositing sufficient energy in a microcircuit's sensitive region to increase or decrease the associated logic's voltage beyond the technology threshold [1]. Based on the duration of the faults in semiconductors, these events are categorized in three main groups, namely, transients, upsets and latch-ups. Single-Event Transient (SET) may lead to a loss of information, physical failures or, in the worst case, to a total loss of function of the circuit. In critical systems like spacecrafts this kind of failure can cause failing of the mission. Single-Event Upset (SEU) is simply the unintentional switching of a digital logic state following an ion strike. Single Event Latch-ups (SEL) are the most serious of the single event phenomena since they possess the potential to permanently damage a device. To evaluate the performance of the electronic devices in the space environment, some ground tests should be conducted to determine the level of immunity against environmental stimulus and to predict the rate of failure for each device. Two main facilities used for this kind of tests are heavy ion facilities and laser laboratories. Due to the availability of laser facilities and some other technical advantages, this method has been chosen for studying the hardness of a microcontroller in the space environment. In this paper, first the space environment and the main expected effects on semiconductor devices will be presented. Then, we will describe the laser test method for single event effects. In the last se ction the test procedure and the results will be explained. Based on the results achieved, the criteria for improving reliability of the system at the component level, board level and system level will be identified.