SPACE SYSTEMS SYMPOSIUM (D1)
Lessons Learned in Space Systems (5)

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DESIGN AND RELIABILITY ANALYSIS OF HETEROGENEOUS FAULT-TOLERANT ON-BOARD COMPUTER FOR MICRO-SATELLITES

Abstract

This paper proposed a low-cost, high performance heterogeneous on-board computer (OBC) system developed by BUAA that has the fault-tolerant capability working in the harsh space environment. OBC hardware is designed by the dual cold backup processor unit (PU) plus arbiter unit (AU) hybrid scheme.Firstly, single processor unit (PU) hardware design based on ARM7, software architecture based on real-time operating system (RTOS) and arbitration mechanism based on 3-level watchdogs are given, and error detection and correction (EDAC) circuit based on FPGA are discussed to protect SRAM cells against single event upset (SEU). Secondly, the heterogeneous fault-tolerant strategy is presented detailed. Thirdly, the OBC system reliability analysis has been done. OBC software architecture is described. The software is running on the RTEMS, which is an embedded real-time operating system. it includes the application tasks module, task schedule module, service function module, RTEMS(RTOS kernel) and boot and emergency management program. The OBC system can work on both the health mode and degradation mode. The reliability analysis and OBC system test results show that the heterogeneous fault-tolerant space OBC system based on COTS could meet the requirements of the low-cost, sustainable micro-satellite missions.