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A NOVEL ACQUISITION ARCHITECTURE FOR MULTI-MODE SATELLITE NAVIGATION SYSTEM RECEIVER BASED ON CORDIC ALGORITHM

Abstract

Acquisition is one of the main function modules of the baseband system of satellite navigation receiver, and the key units of the acquisition module are the correlation processing unit for chip searching and the FFT unit for frequency searching. As the parallel code phase search based on FFT can acquire not only the code phase shift but also the Doppler frequency shift of the carrier signal at the same time, it has been widely used in GNSS receiver. However, in the multi-mode satellite navigation system receiver, some defects appear in the application of the parallel code phase search algorithm. The lengths of sampled data in different satellite navigation systems are different, then the lengths of FFT in different navigation systems can't be expressed by the 2's integer power at the same time, so the realization of FFT processor can't complete the FFT operation in this condition. Under this situation, a conventional method is adding 0 by the following of the sampled data. The shortcoming of this method is that we must increase the length of the FFT processor, it will lead to more hardware consumption and higher power. But in many receivers, especially the hand-hold receiver, reducing the hardware consumption and depressing the power is very critical. In a multi-mode satellite navigation receiver, in order to acquire the GPS, GLONASS and COMPASS navigation signals at different chip rates, three different FFT processors are needed when using the parallel code phase search algorithm, it further increases the consumption of the hardware. In order to reduce the hardware and the power consumption, a novel acquisition architecture for multi-mode satellite navigation system based on CORDIC algorithm is proposed. In this architecture, the sampled data are converted into 1024 through a down sampling module, which can reduce the length of the FFT effectively, and the twiddle multiplications are performed by CORDIC-based multipliers, it avoids the hardware multiplier which always occupies a lot of hardware resource. Besides, by using the CORDIC algorithm, the memory resource is also reduced respectively. The experiment results show that the proposed acquisition architecture can greatly reduce the hardware and the power consumption while keeping the fast acquisition. The hardware resource and the power consumption in the proposed architecture are 62.5% and 60.9% respectively compared with the conventional algorithm, which may be attractive for the mutli-mode satellite navigation system receivers.