

47th SYMPOSIUM ON SAFETY, QUALITY AND KNOWLEDGE MANAGEMENT IN SPACE  
ACTIVITIES (D5)

Ensuring quality and safety in a cost constrained environment: which trade-off? (1)

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## DOES YOUR TEST BENCH REFLECT REALITY?

**Abstract**

Years of experience in Assembly, Integration and Verification of space systems have taught the authors valuable lessons for setting up and assessing space system test benches. One of the most important lessons has been that a test bench is often misused. We found that when creating a test bench to perform verification and validation of a space system, design decisions have to be made to include or exclude certain functionality aspects of the future operational system. The complete test bench is therefore only a reflection of reality, and tests performed (or results expected) do not match the capabilities of the test bench.

## Test Bench Design Choices

During system design, as the requirements are flown down to subsystem level and below, the verification programme is designed to verify all requirements at all levels. With every requirement that is flowed down, a design decision is made. The same thing happens when creating the test bench: every stub and every test tool is based on design decisions. So we need to look into the choices we make during design of the test bench, and question our awareness of these choices. How do we write test bench requirements? Are the requirements directly related to coverage of system requirements, or are they a functional representation? How do we define test tools?

## Making a test bench that meets the program's needs

During the definition phase of a test bench, the (sub) system under test must be defined and limited. Decisions need to be made where to use a tool, where to use a real subsystem, and where to make the interface between the (sub) system under test and the wider world. This is in turn influenced by how well a test tool can simulate reality: a vacuum can fairly easily be created, launch vibrations are regularly simulated, but where do we define the interface between item under test and test bench in case of an S-Band communication chain?

## Impact of Test Bench Design on System Test Reliability

Each test bench design decision is taken with cost/benefit in mind; The whole AIV process exists to lower system costs by lowering risks. So, the environment in which the test bench is designed is one in which the cost of system risks is known (or estimated), and the reality level of the test bench must be matched with the calculated level of acceptable risk.