22nd IAA SYMPOSIUM ON SMALL SATELLITE MISSIONS (B4) Generic Technologies for Nano/Pico Platforms (6B)

Author: Prof. Diego Barrettino Scuola Universitaria Professionale della Svizzera Italiana, Switzerland

A SUPERCOMPUTER FOR PICO-SATELLITES

Abstract

This paper presents the design and development of a supercomputer for pico-satellites (printed-circuit board size 10 cm x 10 cm) comprising eight computing units (Gumstix modules), two reconfigurable routers and all the necessary peripherals. The supercomputer architecture takes into account the typical failures in space environment (for example, Single Event Upset) by implementing a triple-redundant hardware configuration where three computing units process the same task at a given time, which can detect an error after a failure and discard it. The reconfigurable router implemented with a field-programmable gate array (FPGA) handles the interconnections among the computing units, the exchange of data among the computing units (via the general-purpose memory controller protocol) and the exchange of data with the external world (via Ethernet). The reconfigurable router is replicated using a second FPGA in order to provide a backup in case of failure resulting in an increase of the supercomputer reliability. Ground-based experimental results show that this supercomputer is capable of processing up to 16,000 MIPS, can store up to 512 GB of data and has a maximum power consumption of 10 Watts when all computing units are operating in parallel. In addition, some Gumstix modules are now under radiation tests in the International Space Station (ISS) and the results of these tests will be probably available in early 2015. This supercomputer is planned to be used for the on-board signal processing of the Micro Solar-Flare Apparatus, which is a compact X-ray detector mounted on a 6U pico-satellite and designed to obtain qualitatively new information about solar flares by providing multidirectional observations of their X-rays.