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# REAL TIME FAULT TOLERANT DESIGN OF RF CMOS PHASE LOCKED LOOP DESIGN FOR RADIATION ENVIRONMENT

**Abstract**

This research work proposes a highly reliable, stable clock source for high frequency applications to address the proliferation in the communication standards due to the growing demand of data transmission within the domestic and commercial market. The necessity of higher data rates, size and the congestion of the radio spectrum have caused the migration of the newest Broadband Wireless Standards up to higher frequency bands. The 60GHz band has recently been allocated worldwide for unlicensed wireless communications systems. It's now likely that 60GHz will become the next big frequency in wireless world, with both short-range and wider area applications. The phase locked loop (PLL) has become the standard solution for the implementation of frequency synthesizers, which is used to generate high frequency stable clock signals for time critical Real Time Systems. PLL circuits have been identified as the single event soft point in space and military electronic systems, their reliable operation is of critical importance. In order to achieve high stability, special techniques are needed to "harden" the circuit against radiation. Radiation Hard low cost fault tolerant solution is need of the hour. Hence this paper is proposing to adopt Radhard design approach which has low cost against Radhard process approach. So the author proposes a novel design approach for PLL to reach a target frequency of 60GHz. This PLL design is challenging since it has a combination of several building blocks with different characteristics covering the entire spectrum of circuit design: analog, RF, mixed- signal and digital. This PLL shall be suitable to use in systems working in radiation environment.