66th International Astronautical Congress 2015

45th STUDENT CONFERENCE (E2)
Educational Pico and Nano Satellites (4)

Author: Mr. Vaibhav Rekhate
College of Engineering Pune, India, rekhatevm11.comp@coep.ac.in

Mr. Abhishek Joshi
College of Engineering, Pune, India, joshiab11.comp@coep.ac.in
Mr. Pritesh Chhajed
College of Engineering Pune, India, chhajedpv11.extc@coep.ac.in
Mr. Nikhil Sambhus
College of Engineering Pune, India, sambhusnp11.comp@coep.ac.in
Mr. Sendhilkumar Alalasundaram
College of Engineering, Pune, India, alalasundarams11.extc@coep.ac.in
Mr. Abdulhussain Songerwala
College of Engineering, Pune, India, songerwalaaq12.extc@coep.ac.in
Mr. Dhaval Waghulde
College of Engineering Pune, India, dhavalvw12.extc@coep.ac.in
Ms. Rucha Vaidya
College of Engineering, Pune, India, vaidyars12.comp@coep.ac.in
Mr. Sayed Umair Daimi
College of Engineering, Pune, India, daimisu13.comp@coep.ac.in

DESIGN, IMPLEMENTATION AND INTEGRATED TESTING OF HARDWARE AND SOFTWARE INTERFACES BETWEEN SUBSYSTEMS IN A PICO SATELLITE

Abstract

Developed by undergraduate students from College of Engineering, Pune, 'SWAYAM' is a 1U class communications satellite anticipating a favorable launch window from ISRO (Indian Space Research Organization). SWAYAM hosts three active subsystems viz. Communication, On-board Computer (OC) and Electronic Power System (EPS), out of which, OC and Communication have their own microcontrollers with fixed set of functions. The EPS being an analog system consists of a load protection circuitry at its core which handles all possible voltage and current contingencies that may arise during satellite operation. The OC houses the satellite's Operating System and File System, and the Terminal Node Controller (TNC) on Communication system primarily manages Digital Communication.

The OC and TNC communicate among themselves in several scenarios such as Antenna Deployment, Periodic Beacon Transmission, Communication Handling, and Satellite Lifetime Management. Streamlining the relay of data between the two controllers introduces several challenges such as Data and State Consistency, Byte Synchronization, Recovery from Down Time etc. As the central computing unit of the satellite, the OC monitors power loads by interfacing with the load protection blocks in EPS. To perform this task, faults are conveyed to the OC through hardware interrupt lines (acting as "fault lines"), following which the OC employs a time-based remedial solution, backed by an algorithm specifically designed to safeguard the crucial components of the system.

With such diverse systems and modules, an intelligent design of the interfaces - both on the hardware and software fronts - holds paramount importance. Moreover, individual and integrated stress testing of this arrangement for every conceivable case holds great significance, and plays a crucial role in guaranteeing impeccable functioning of the integrated system as a whole. This paper explains the design and implementation of the interface between the two controllers and their working in conjunction with a load protection logic, modeled to ensure modularity, robustness and fault tolerance. This paper then delineates the module-wise and integrated testing sequence implemented to secure maximum reliability of SWAYAM.