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A NOVEL IMPLEMENTATION OF BEACON RECEIVER USING FPGA

Abstract

Beacon receiver is an important part of the ground segment in satellite technology. This paper presents a software defined radio based digital beacon receiver. The beacon receiver is developed on Xilinx FPGA. The objective of the project was to develop a cost effective solution with good power estimation accuracy. In order to achieve this goal the direct IF digital processing strategy is used, this allows eliminating the preprocessing requirement resulting in saving DSP resources. Around 55