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TWO TYPES OF RADIATION HARDENED SOCS FOR SATELLITES APPLICATION

Abstract

Radiation hardened design cost and radiation hardening assurance are the main concerns of spaceborne electronics. Because of the financial and time limits, it is a better choice to harden the design in circuit and architecture level or above, rather than semiconductor device level. Meanwhile, due to the volume, weight and power restrictions, much of the onboard electronics have been integrated into a single die, namely SoC (System on Chip). In this paper, two types of spaceborne SoCs are proposed. The first one is a multicore CPU (Central Processing Unit) with eight RISC-like processors and several peripherals, such as SPI, PWM, etc, integrated into a single die. The second one is a customized special purpose controller with special voltage requirement on output pins, which is formerly realized with an reconfigurable FPGA device. Approximately, the former one is 100K gates scale design, while the last one a few kilo-gate. This paper gives a brief review of the radiation hardening strategies and chooses the appropriate hardening methods to these two different scale electronics with the consideration of area, power dissipation and financial and mission schedule. As the technology shrinking into deep-micron scale, the probability of soft error induced by SET to combinational logic and SEU to registers firstly exceeds the fault probability of the ECC protected memory components. So the radiation hardening assurance is essential to spaceborne electronics design to avoid the overdesign or underdesign. Accelerated radiation tests on these two chips with various applications prove that the chosen radiation hardening methods can meet the requirements of the mission definition. The rich ends of the two projects offer opportunities for further development of smaller and highly reliable avionic electronics on satellites.