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A RADIATION HARDENED MULTICORE DSP PROCESSOR DESIGNED FOR SPACE MISSIONS

Abstract

Single particle effects (e.g, ESU, SET) are a potential threat to the reliability of digital circuits operating in space environment, especially when the sub-micron commercial semiconductor technology (65nm or below) has been adopted in spaceborne electronics. SEU&SET are caused by high-energy particles striking into sensitive areas of the device, producing changes in the content of registers and memory elements. Since future space electronics requirements may not be manufactured by incredibly expensive radiation hardened semiconductor technology, the use of commercial off the shelves (COTS) solutions with hardened strategies are proposed. In this paper, a COTS multicore processor, namely Revealer1601p, with different abstraction levels hardened strategies against SET and SEU, is designed for space missions. Due to the cost of full hardening (such as Triple Module Redundancy, TMR), an analysis to components and circuit level proves that partial hardening can obtain the demanding reliability based on radiation tests on various space applications. Compared with the typical TMR, a 63.6% hardware cost reduction is achieved. The SEU error rate is $\leq 1e-5 Error/device{\cdot}day$. The full paper first gives a brief introduction to the processor architecture. Then a detailed discussion of the strategies adopted to different components is presented and a software/hardware cooperating strategies for reliability is also discussed. We conclude this paper with fault injection test and some interesting results of the SoC level FIT (Failure in Time) rate are obtained.