Paper ID: 33288
oral
student

MATERIALS AND STRUCTURES SYMPOSIUM (C2)
Specialised Technologies, Including Nanotechnology (8)

Author: Mr. Hui Cao
Xi'an Microelectronics Technology Institute, China Aerospace Science and Technology Corporation (CASC), China

Dr. Liang Yang
Xi'an Microelectronics Technology Institute, China Aerospace Science and Technology Corporation (CASC), China
Mr. Fei Yu
China
Mr. Weiqiang He
China

REVEALER1601 - A MULTIPLE-CORE DIGITAL SIGNAL PROCESSOR FOR DEMANDING SPACE APPLICATIONS

Abstract

The Revealer1601c integrated circuit is a first of its kind, offering high-performance orbital processing ability to ultra-high resolution multiple spectra images. With the consideration of reliability, flexibility and availability, the device is a System-on-Chip implementation, integrating various processors, high-speed data transfer controller and memory controllers on a single die. The device is highly configurable and can be applied to space tasks ranging from control and data processing.

The main functions of the revealer1601c processor are:

1× PowerPC470 Processor as the master processor

15× RISC-like, SIMD architectural 32-bit Digital Signal Processors as synergistic processors (SP)

360× Computational Accelerating Engines

Continuous Streaming Processing Engine (CSPE) for each SP

IEEE-754 and 40-bit extended precision Floating Point Unit for each SP

4 × 16KByte Instruction Cache and 4 × 16Byte Data Cache for each SP

Shared Logic for Design for Test (DFT) and Debug support for all on-chip IP-block with JTAG interface

Fault-tolerant Network on Chip (NoC) connecting all IP-blocks

4X RapidIO controllers with each having a data transferring speed of 25Gbps

Memory controller for DDR2/DDR3/QDR memory with physical layer radiation hardening

Low Power Management Unit (LPMU) and peripherals such as Timers, UARTs, Interrupt controller

The device can run at 400MHz system clock frequency and is expected to approximately achieve a performance of 102.4 GMACS and 51.2 GFLOPS. The Revealer1601c is fabricated at SMIC Ltd. commercial semiconductor foundry, using standard 65nm CMOS technology. It employs architecture and software level radiation-hard methods for reliability.

As a preparation for R&D, a silicon prototype, the Revealer0401, integrated with 4 processors and peripherals has been successfully manufactured , validated and applied in mission deployment. As its predecessor, the Revealer1601c device will soon be applied to the high resolution SAR imager system prototype as the primary onboard calculation accelerator. With the links of RapidIO, several devices can be meshed together to be a homogeneous computing array, offering Tera-FLOPS (10^{12} Floating Point Ops Per-Second) level computing ability.

The full paper will provide an overview of the Revealer1601c processor, its various function units and the primary applications in space domain. It will also be discussed the mitigation techniques adapted against space radiation effects, encompassing both the design methods and radiation assurance test results.