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FPGA IMPLEMENTATION OF A HIGH THROUGHPUT ERROR CORRECTING TELE-COMMAND DECODER

Abstract

The paper provides the implementation of the CCSDS suggested (63, 56) BCH code for tele-command decoder. The (63, 56) code is a modified BCH code which has the advantage of Single Error Correction and Double Error Detection (SECDED). The implementation is memory efficient, has high throughput and zero latency. On an FPGA it is implemented by the use of Look-Up Tables (LUTs). The LUTs are generated based on the specific generator polynomial of the code being used. The working principle behind the implementation is to store the GF (64) elements of the Parity Check Matrix as binary vectors. By doing so the matrix multiplication gets reduced to binary multiplication. This reduces the logic gates utilization in the FPGA.