Small Satellites (13)
Small Satellites (2)

Author: Mr. Abhishek Goel
Birla Institute of Technology and Science(BITS), India, abhigoel1996@gmail.com

Mr. Saurabh Raje
Birla Institute of Technology and Science(BITS), India, f2015045@pilani.bits-pilani.ac.in
Mr. Shubham Sharma
Birla Institute of Technology and Science(BITS), India, shubhamsh695@gmail.com
Mr. Dhananjay Mantri
Birla Institute of Technology and Science(BITS), India, f2015139@pilani.bits-pilani.ac.in
Mr. Kushagra Aggarwal
Birla Institute of Technology and Science(BITS), India, kushagra.aggarwal01@gmail.com
Mr. Tanuj Kumar
Birla Institute of Technology and Science(BITS), India, kmrtnjscnc@gmail.com

A NOVEL DESIGN FOR ON-BOARD SOFTWARE FOR A NANOSATELLITE

Abstract

A group of undergraduate students from BITS-Pilani are building a nanosatellite whose objective is to perform hyperspectral imaging of the Earth's surface. This has never been carried out by a nanosatellite due to constraints on power generation and transmission rate. This paper describes the process of conceptualization, design and testing of a novel implementation of the Onboard Computer Flightplan for a 3U nanosatellite. The on-board computer of the satellite is responsible for controlling the activities of all other subsystems, controlling dataflow between onboard hardware and performing important computations like image compression. The software computation to be done by the onboard computer will be implemented on a Linux based operating system run on the ARM Cortex A9 processor which is part of the Zynq-7000 SoC. A Field Programmable Gate Array (FPGA) will be used specifically for image compression which after compression will be stored in a serial flash memory shared between the camera and the FPGA. The architecture comprises of a system-wide I2C bus to which various sensors like magnetometer, temperature sensor, IMU etc. are interfaced. The collected data will be used for housekeeping and as inputs to algorithms used for pointing and detumbling. An SPI interface is used between the Power Subsystem microcontroller and the On-Board Computer since a large amount of housekeeping data will have to be exchanged at high rates. Also actuators namely, reaction wheels and magnetorquers are actuated by current driver circuits which get the control signals from the OBC. We have divided the functioning of the satellite into modes, each of which is represented by a linked-list whose nodes represent the tasks to be performed periodically when the satellite is in that mode. Each task has a predefined first time of execution and next time of execution, and the linked list is ordered by the next time of execution. A background process called Flight-plan runs oversees the execution of the tasks in the linked list of a mode based on the system time and next time of execution. The functions represented by the linked lists have been written in an optimally parallelized way to increase throughput. The Flightplan also responds to critical situations which is monitored by the housekeeping data received. We review some common fault detection, isolation and removal methods and their software implementation and describe our architecture and discuss related implementation issues in this paper.