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A SERIES OF SOC DESIGNS FOR SPACE APPLICATIONS

Abstract

In current and ongoing space explorations, electronics play an essential role in the near-earth activities and deep-space missions. This paper presents a series of system on chip (SoC) designs for space applications. The first SoC is an application specific integrated circuit (ASIC) designed for the multi-channel remote testing signals transferring. The chip has been packaged into a system in package (SiP) module to replace the former PCB level signal processing system with two SRAM-FPGAs for redundancy design. Hence greatly reducing the weight, volume and power. The second SoC is a multi-core controller designed as the central processing unit in a multiple tasks control application, which has eight low power, real time processing cores. The processor has been hardened to immune the signal event effects (SEEs). The last proposal is a high performance digital signal processor (DSP) designed for obtaining orbital massive data processing capability. Each core in the DSP is a single instruction, multiple data (SIMD) stream processing accelerator to meet the peta floating point operations per second (PFLOPS) level calculating ability. Each core has a reconfigurable streaming processing engine (SPE) to satisfy various data-intensive tasks. Meanwhile, for reliability consideration, the DSP is hardened with flexible strategy, which can be configured to run in a normal mode or reliable mode. The three kinds of SoCs represent three different application domains in space. In the full paper, the similarities and differences of the design philosophy, reliability consideration, manufacturing flow and miniaturization, power and performance compromising will be discussed in the full paper and conclusions will also be given on how to choose design strategies to meet the mission requirements.