Paper ID: 37264
student

Poster Session (P)
Poster Lunch (1)

Author: Dr. Hui Cao
Xi'an Microelectronics Technology Institute, China Academy of Space Electronics Technology (CASET), China Aerospace Science and Technology Corporation (CASC), China, caoyh6@163.com

RECENT PROGRESSES ON RADIATION EFFECTS IN ELECTRONICS AND THE APPLICATIONS OF VARIOUS MANUFACTURING TECHNOLOGIES FOR RELIABILITY IN SPACE ELECTRONICS

Abstract

Electronics exposed into space environment will suffer from various radiation effects impacting the reliability of the system. Meanwhile, a major trend is that most satellites venders benefit commercial off the shelves (COTS) hardware and software for agile manufacturing and testing. Hence the susceptibility of such spacecrafts in orbits comes to be prominent threat. For sophisticated designers, the most concern is to know the characteristics of radiation effects from the perspectives of devices and integrated circuits so as to apply appropriate hardening techniques for a reliable design. As semiconductor manufacturing technology shrinking to sub-micron metrics and the application of new geometry structures, the radiation effects in such technology nodes represent some new characteristics than what has been historically observed for conventional regions. This paper surveys the recent progress of radiation effects researches on state-of-art semiconductor manufacturing processes, including SOI and FD-SOI, bulk planar CMOS and FinFET or 3D Tri-gate technologies ranging from 45nm to 12nm. With the emphasize on chip level integrated circuits (ICs), we classify the most commonly used chips in spacecrafts into two categories, that is, memory ICs, including flash memories, SRAM and stacked SRAM, DRAM and EEPROM, an logic ICs, including processor, SRAM- and FLASH- based FPGA and application specific integrated circuits (ASICs). The memory ICs are highly vulnerable to multicell upset (MCU) resulted by single event effect (SEE) at advanced technology nodes due to the close placements of the storage cells. It is recommended to the designer to pay attention to MCU problems and attach protection to memory ICs. Compared to memory ICs, logic ICs have more chances to mask the SEE errors, thus having more opportunities to be protected. In this paper, the vulnerability estimating methods will be also discussed for the further evaluation to ICs. Finally, the radiation hardening assuring techniques are investigated to guide a reliable design. This survey represents a brief description of radiation effects to state-of-art semiconductor technologies and offers a primary guidance for the spacecrafts designer to choose appropriate COTS or hardened devices in their designs.