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SPACE SYSTEMS SYMPOSIUM (D1)
Technologies to Enable Space Systems (3)

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A SERIES OF SPACEBORNE SOC DESIGNS FOR SPACE APPLICATIONS

Abstract

In current and ongoing space explorations, electronics play an essential role in the near-earth activities and deep-space missions. Due to the volume, weight and power constrains, the former PCB based onboard electronics has been integrated into a single device in planar or 3D-stacked packaging, namely SoC (System on Chip). This paper presents a series of SoC designs for space applications.

The first SoC is an application specific integrated circuit (ASIC) designed for the multi-channel remote testing signals transferring. The chip is a 100K gates scale design and is fabricated using 0.5μm SOI (Silicon On Isolator) semiconductor process. The chip has been packaged into a system in package (SiP) module to replace the former PCB level signal processing system which has two SRAM-FPGAs for redundancy design. Hence greatly reducing the weight, volume and power. The SiP module has been packed in an geosynchronous orbit satellite and worked well for months.

The second SoC is a multi-core controller designed as the central processing unit in a multiple tasks control application, which has eight low power, RISC-like processors. The processor has been hardened to immune the signal event effects (SEEs). The processor is fabricated using commercial 180nm standard process and can run 125MHz at 3.3 voltage.

The last proposal is a high performance digital signal processor (DSP) designed for obtaining orbital massive data processing capability. Each core in the DSP is a single instruction, multiple data (SIMD) stream processing accelerator to meet the peta floating point operations per second (PFLOPS) level calculating ability. Each core has a reconfigurable streaming processing engine (SPE) to satisfy various data-intensive tasks. Meanwhile, for reliability consideration, the DSP is hardened with flexible strategy, which can be configured to run in a normal mode or reliable mode. The DSP is manufactured on commercial 65nm process with particular hardening on the layout of the library cells and can run 400MHz at 1.8V.

With the constraints on finance and mission schedule, it is a better choice to harden the SoCs in architecture level or above, rather than semiconductor process level. The three kinds of SoCs represent three different application domains in space. In the full paper, the similarities and differences of the design philosophy, reliability consideration, manufacturing flow and miniaturization, power and performance compromising will be discussed and conclusions will also be given on how to choose design strategies to meet the mission requirements.