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REVEALER-FT : DESIGN OF A FAULT TOLERANT DIGITAL SIGNAL PROCESSOR FOR SPACE MISSIONS

Abstract

The tendency of continuous requisite for computation power in space missions, coupled with the high reliability and the miniaturization of feature size and power dissipation, has triggered the development of a new generation spaceborne processor architecture seeking high computation efficiency. Typical expeditions include NASA's Maestro project of developing a 49-core high performance radiation hardened processor for future space mission and ESA's SSDP (Scalable Sensor Data Processor) program targeting a new data processor beyond the conventional LEON/SPARC architecture. Under the project of Ultra-high Resolution Orbital Data Processing, we have developed a new highly parallel streaming processor architecture, namely Revealer-FT, which can be usable standalone or as a building block in a MultiProcessor System-on-Chip (MPSoC).

In this paper, the microarchitecture and implementation of the Revealer-FT is presented. Revealer-FT features a RISC-like, a 4-way SIMD architecture with streaming accelerating engine. To speedup the processing capability, several innovations have been involved into the architectural design. Featuring a 13 stage pipeline, the core claims the first a non-fixed instruction pipeline together with a flexible hazards settlement mechanism in static scheduling to pipe out flying instructions as soon as possible to remove stalling penalty. A non-interlocked streaming process mechanism and easy programmable code patterns are proposed to accelerate massive data continuous processing. For reliability consideration, the processor tolerates SEU (single event upset) faults by using transparent SEU mitigation techniques such as TMR (triple module redundancy) registers, parity checking, EDAC code. In addition, several innovations have been involved for flexibility and availability with minimal overhead, such as multi-level memory refreshing, programmable data refreshing and multiple data processing lanes redundancy.

A prototype of Revealer-FT is manufactured on a commercial-off-the-shelf (COTS) 65nm CMOS process with particular hardening design on the COTS memory library. The core size is about $3013\mu\text{m}\times3011.5\mu\text{m}$. With a 1.5V power supply, the core can run at 400MHz with a performance gain of 3.2GFLOPS while the power dissipation is 0.85mW. The heavy-ion injection and low energetic ions injection tests are carrying out to evaluate the threshold for single event upset (SEU) and total-ionizing dose(TID). The soft error rate is expected to be less than $1e-5 Error/device{\cdot}day$.

The full paper will propose the detailed design of this portable processor. The comparison with other fault tolerant processor will also be given and a discussion shows that the Revealer-FT has a better performance-energy efficiency than others.