45th STUDENT CONFERENCE (E2)
Educational Pico and Nano Satellites (4)

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DEVELOPMENT OF ON BOARD COMPUTER FOR A NANOSATELLITE

Abstract

A group of undergraduate students from BITS-Pilani are building a nanosatellite whose objective is to perform hyperspectral imaging of the oceans. This has never been carried out by a nanosatellite. The spectral distribution shall help in categorizing various phytoplankton in the oceans. This is used to study the carbon cycle of the oceans, which has an impact on the marine life. This paper describes the process of conceptualization, design and testing of the Onboard Computer (OBC) Software for a 3U nanosatellite. The on-board computer of the satellite is responsible for controlling the activities of all other subsystems, initiating dataflow between onboard hardware and performing mission critical computations like image compression. Control algorithms for fine pointing, sun pointing, ground pointing for payload operation and idle state detumbling run on the on the OBC. The actuation associated with this is carried out by interfacing magnetorquers and reaction wheels with the OBC. The software of the onboard computer is implemented on a Linux based operating system run on the ARM Cortex A9 processor which is part of the Zynq-7000 SoC. A Field Programmable Gate Array (FPGA) is used specifically for image compression. The compressed image is stored in a serial flash memory shared between the camera and the FPGA. The architecture comprises of a system-wide I2C bus to which various sensors like magnetometer, temperature sensor, IMU etc. are interfaced. The collected data is used for logging followed by downlink, and as input to algorithms used for pointing and detumbling. An SPI interface is used between the Power Subsystem microcontroller and the On-Board Computer since a large amount of housekeeping data will have to be exchanged at high rates. Also actuators namely, reaction wheels and magnetorquers are actuated by current driver circuits which get the control signals from the OBC. The satellite is modelled as a Finite State Machine for software development. The states broadly fall under two categories, Normal and Emergency. Each state has a predetermined set of logical tasks to be run, which are abstracted as separate processes in the memory. State transitions take place by polling the health metrics of the satellite. However, hardware interrupts are implemented on selected peripherals which ensure a asynchronous switching to Emergency States for safety. Details of hardware in loop simulation for the breadboard model of the satellite are included. A review of some common fault detection, isolation and removal methods used shall conclude the paper.