Paper ID: 43473
oral
student

IAF SPACE SYSTEMS SYMPOSIUM (D1)
Technologies to Enable Space Systems (3)

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PROBLEMS, CHALLENGES AND EXPERIENCES FROM SEVERAL PRACTICAL SOC CHIPS FOR SPACEBORNE ELECTRONICS

Abstract

This paper has surveyed four VLSI(Very Large Integrated Circuits) chips design dedicated for diverse space applications. These designs range from FPGA-to-ASIC designs with hundreds of kilo-gates to digital signal processor (DSP) heterogeneously integrating 17 processors for Giga-FLOPS computing capability. These chips typically cover the main electronics in our already launched and future deploying space missions. In current and ongoing space explorations, spaceborne electronics play an essential role and proposed here are a series of system on chip(SoC) designs for such demandings.

The first proposal is an application specific integrated circuit (ASIC) designed for the multi-channel remote testing signals transferring. The chip has been packaged into a system in package (SiP) module to replace the former PCB level signal processing system with two SRAM-FPGAs for design. Hence greatly reducing the weight,volume and power.

The second chip is an FPGA-to-ASIC design that replaces the previous realization on a four anti-fused FPGA system board. This chip will be deployed in a remote sensing satellite. Various fault tolerance techniques are adopted to fight against the radiation effects with the same or exceeding ability as the intrinsic radiation immunity of anti-fused FPGA.

The third is a multi-core controller designed as the central processing unit in a multiple tasks control application, which has eight low power, real time processing cores. The processor has been hardened to immune the signal event effects(SEEs).

The last proposal is a high performance digital signal processor (DSP) designed for obtaining orbital massive data processing capability. Each core in the DSP is a single instruction, multiple data (SIMD) stream procesing acelerator to meet the peta-FLOPS(Floating Point Operations Per Second) computing capability. Each core has a reconfigurable streaming processing engine (SPE) to satisfy various data-intensive tasks. Meanwhile, for reliability consideration, the DSP is hardened with flexible stategy, which can be configured to run in a normal mode or reliable mode.

All these kinds of SoCs represent different applications domains. In the full paper,the similarities and differences of the design philosophy, reliability consideration ,manufacturing flow and miniaturization,

power and performance compromising will be discussed and conclusions will also be given on how to chose design stategies to meet the mission requirements.