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CLOCK SYNCHRONIZATION ONBOARD A CONSTELLATION OF SMALL EARTH OBSERVING LEO SATELLITES

Abstract

In a constellation of small earth observation satellites that gathers data regarding some physical terrestrial phenomenon such as weather, measurements need to be time-stamped in order for them to be meaningful for further interpretation. Such a feature could be implemented by equipping each satellite with a real-time clock (RTC), or if higher accuracy is required, a GPS receiver. For applications requiring an even higher level of synchronization accuracy, or where access to a GPS receiver is unavailable, clocks onboard constellation satellites could be synchronized using direct inter-satellite links. This paper describes one such method for clock synchronization onboard LEO satellites.

Contrary to most communications, networking, or broadcast applications where clock synchronization is achieved by tracking a certain upstream master clock, our method uses a consensus building approach to clock synchronization among constellation satellites. The advantages of such an approach lie in its robustness in case of a satellite link failure or a total satellite failure. The difficulty in realizing such an approach though comes from the fact that instead of taking the frequency and phase of a single master clock into consideration, multiple clocks need to be considered in order to derive the synchronized clock. Additionally, the delays of the inter-satellite links must also be factored into the synchronization process.

In this research firstly we adapt the feedback control loop of a traditional phase locked loop (PLL) to our collective clock synchronization problem. Then we show the results of simulations depicting the performance of this proposed system. Next, we implement the digital control loop portion of the design in an FPGA, and show that the required logic resources are small enough for several instances to fit onto a single COTS FPGA board. We realize the design on a low-end COTS FPGA board, and connect the board to several off-board voltage controlled crystal oscillators (VCXOs) using wire harnesses. The VCXOs act as the clock sources that are to be synchronized onboard the constellation satellites. We emulate various satellite link delays within the FPGA, and evaluate the quality of our clock synchronization under different scenarios. Additionally, we emulate for various fault conditions such as single to multiple VCXO failures, and determine their effect on the performance of the overall system. Finally, we conclude with outlining the applicability and limitations of such a clock synchronization scheme to various Earth observation small LEO satellite constellation missions.