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Author: Ms. Adilson Barbosa
National Institute for Space Research - INPE , Brazil, eng.adilsonlb@gmail.com

Dr. Geilson Loureiro
National Institute for Space Research - INPE , Brazil, geilson@lit.inpe.br
Dr. Silvio Manea
Brazilian National Institute for Space Research - INPE, Brazil, silvio.manea@inpe.br
Dr. José Duarte
National Institute for Space Research - INPE , Brazil, jose.duarte@inpe.br
Dr. Giuliani Garbi
National Institute for Space Research - INPE , Brazil, giuliani.garbi@gmail.com

MITIGATION OF COTS FPGA FAILURES CAUSED BY RADIATION EFFECTS

Abstract

This article presents the development and implementation of a structure to assist the systems engineer, considering a process of choosing a fault mitigation technique for a space system with electronic integrated circuits of the type COTS-FPGA (Commercial off-the-shelf - Field Programmable Gate Array). Space systems require spatially or hard-qualified components, and some applications also require devices with a high processing rate, low power consumption, and low cost. The studies surveyed in the available literature, over a ten-year period, didn't provide sufficient design details to compare existing mitigation techniques in a manner consistent with the required parameters. The technique selected should ensure that the FPGA of the electronic device works properly with the mission applications and overcomes the adversities of space, especially the effects of radiation. Due to factors related to the reduction of costs of these projects and the possibility of commercial embargo of hard components, the electronic devices of the type COTS happened to occupy a relevant space in the engineering of components. FPGAs COTs, although not manufactured for the radiation environment, cost up to twenty times less and can absorb, by hardware or software, mitigation techniques. A space project must meet or exceed all mission restrictions such as maximum power usage, maximum failure rate, and minimum required life time. Considering that these restrictions are different and often conflicting, different types of solutions are possible. The paper proposes a study of two frameworks available in the literature, but which present partial results, watertight and without establishing a standard flowchart. These frameworks address separately the two types of radiation effects (TID - Total Ionizing Dose or SEE - Single Event Effects) and only four mitigation techniques. Just only one of the articles presents metrics and methodology for the selection process. This article performs a detailed study on the mentioned frameworks and proposes measures to build a single framework that overcomes the disadvantages of the previous two, such as the consideration of a longer period of research and a greater number of mitigation techniques, among others. With the implementation of these measures, the component engineer can only use this tool for the design of projects in the area of COTS FPGA, with the mitigation of the radiation effects according to the parameters of the mission.
Keywords: COTS-FPGA, fault mitigation techniques, framework, systems engineer