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MULTIFUNCTIONAL SOFTWARE-DEFINED RADIO CHIP DESIGNED FOR SMALL SATELLITE APPLICATIONS

Abstract

Humanity is currently witnessing a modern space race promoted by private companies impelled by cutting-edge technologies and fewer constraints required to access space. This results in the development of reduced-size components and satellites that demand less time from manufacturing to launch. Therefore, all efforts are increasingly focused in achieving compact technologies that match the demanding satellite standards from this Newspace age.

Following this trend within the space communications field, some technological gaps are emerging and waiting to be filled in order to provide compact and robust technologies aligned with current demands that have been pushing forward to increase the level of integration in electronic circuits. Hence, it is now possible to replace a software-defined transceiver tailored to the CubeSat standard by a single chip. Although the main functionality of this transceiver is to offer inter-satellite and ground links in S-band, it is also capable of providing ranging, synchronization, positioning and networking functions. By integrating all components of the transceiver in a single chip, it will facilitate and speed up integration, test and qualifications processes which represent major challenges faced by the ever-evolving small satellite market. In addition, this chip prototype will take into account space agencies requirements so that a final version can be certified to comply with major space standards and withstand the space environment.

Due to the highly complex tasks involved in manufacturing a single transceiver die, the proposed chip consists in a System-in-a-Package enclosing two dies: one regarding the digital and mixed signal

processing module and another for the RF front-end. Integrating the transceiver in a single chip offers the opportunity to formulate an improved architecture that provides communications within a broader frequency spectrum thus enabling its use for different applications. Therefore, the RF front-end of this chip is designed to communicate from 300 MHz to 6 GHz (C band), offering the possibility to perform an external up/down-conversion to/from 40 GHz (Ka band).

This paper presents a high-level architecture of the chip detailing all modules and components required to offer the aforementioned functionalities and expected performances. The development process that was defined is also explained and all technical trade-offs are presented to justify the proposed architecture. Additionally, the context around the project is included, both in terms of target applications and certification and qualification of the component for space use.