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Author: Mr. Antonio Latorre
Deimos Space SLU, Spain, antonio.latorre@deimos-space.com

Mr. Francisco Membibre
Deimos Space SLU, Spain, francisco.membibre@deimos-space.com
Mr. Juan Ignacio Bravo
Deimos Space SLU, Spain, juan-ignacio.bravo@deimos-space.com
Dr. Robert Hinz
Deimos Space SLU, Spain, robert.hinz@deimos-space.com
Dr. Alexis Ramos
Deimos Space SLU, Spain, alexis.ramos@deimos-space.com
Dr. Murray Kerr
Deimos Space SLU, Spain, murray.kerr@deimos-space.com

ON-BOARD LOW LATENCY PROCESSING OF EARTH OBSERVATION PRODUCTS IN A MULTI-BOARD SCHEME USING MULTI-CORE AND FPGA-BASED ARCHITECTURE

Abstract

This paper presents the implementation and verification of the EO-ALERT optical product processing chain. EO-ALERT (http://eo-alert-h2020.eu/) is a European Commission H2020 project coordinated by DEIMOS Space, where the main objective is to provide a very low latency (<5 minutes) Earth Observation service globally. This is achieved by processing satellite sensor data on-board the flight segment, to obtain derived products, such as alerts in ship detection and extreme weather applications, which can be transmitted via global communications links. This on-board processing is achieved through efficient use of novel and advanced technologies, including spin-in from other sectors, such as advanced SRAM Multi-Processor and FPGA (Zynq^{TM} UltraScale+^{TM} MPSoC from Xilinx®), multi-board reconfiguration, use of COTS Software for advanced processing or rapid-development (Linux OS, SDSoC^{TM} from Xilinx® or OpenCV libraries) and high-speed PCIe® interfaces.

The HW architecture allows for 1 to 4 boards, in a master slave configuration, to be used for this on-board processing, with them a variable-size target area, thus reducing the total latency of the product generation. On each board the processing takes advantage of the board's resources (multi-core, FPGA) to obtain the processed products and alerts, which are centralised in the master board.

To support the implementation and verification, a PIL (Processor-In-the-Loop) testbench is created. The aim of the test bench is to have a multi-board breadboard representative of the final architecture, where the development performance can be verified. The artificial intelligence (AI) and machine learning (ML) algorithms developed in the project are implemented by migrating them to the target Hardware, taking into account the most efficient implementation on the system multi-core (4 A53 ARM® cores) or FPGA, and the parallelization of processing between the available processing boards. The development includes the use of rapid prototyping tools to produce optimized hardware IP blocks and SW libraries.

The evaluation of the resulting processing system is performed experimentally using real Earth Observation data from a reference-image database, corresponding to the DEIMOS-2 VHR optical satellite and the SEVIRI instrument on the MSG satellite, and therefore the results are highly significative. Ground truth information from multiple sources is used in the verification phase. Furthermore, the performance of the initial algorithms are compared with those obtained in the Hardware, thus obtaining an evaluation

of the effect of the Hardware implementation. The execution times are measured in the PIL platform, obtaining at the present moment results within the requirements (<5 minutes) established in the project.