19th IAA SYMPOSIUM ON SPACE DEBRIS (A6)
Interactive Presentations - 19th IAA SYMPOSIUM ON SPACE DEBRIS (IP)

Author: Mr. Mohamed Salim Farissi
Sapienza University of Rome, Italy

Mr. Ivan Agostinelli
Sapienza University of Rome, Italy
Mr. Marco Mastrofini
University of Rome "La Sapienza", Italy
Prof. Fabio Curti
Sapienza University of Rome, Italy
Mr. Cosimo Marzo
Matera Space Geodesy Center, Agenzia Spaziale Italiana (ASI), Italy
Dr. Claudia Facchinetti
Italian Space Agency (ASI), Italy
Dr. Luigi Ansalone
Italian Space Agency (ASI), Italy

HARDWARE IMPLEMENTATION OF THE SPOT PAYLOAD FOR ORBITING OBJECTS DETECTION USING STAR SENSORS

Abstract

Space debris issue has become an attractive challenge for many applications in the framework of Space Situational Awareness (SSA) and Space Surveillance and Tracking (SST). The Star sensor image on-board Processing for orbiting Objects deTection (SPOT) fits in this field as an innovative space based autonomous and versatile system for Resident Space Objects' optical detection via star sensors and for different Earth orbits scenarios. This system is planned to be a payload for an In-Orbit Validation (IOV) activity in the next future. The purpose of this paper is to show the architecture of the SPOT system together with its implementation on a System on Chip (SoC)/Field Programmable Gate Array (FPGA) space representative board.

The SPOT algorithms involve several layers of filters which are relatively expensive in terms of computational latency, limiting their applicability to real-time image processing applications. Therefore, the filters are well-suited for hardware implementation on FPGA which can dramatically increase the performances by exploiting the parallelism provided by the FPGA. The algorithms are developed and implemented following the Co-Design methodology, the FPGA and CPU work together to share the processing load. In such an approach, FPGA processes the image during few clock periods while CPU controls the data flow and overall operating.This work presents the design and implementation of SPOT algorithm on the Zynq-7000 SoC using Xilinx FPGA and ARM CPU. This technology has been already tested on GOMX-3 and GOMX-4 missions. Algorithms have been modelled with Simulink and implemented on FPGA using Xilinx system generator with aiming to optimize both processing time and area usage.The processing time is reduced by using fixed-point arithmetic while the logic area is reduced by reusing processing elements. Triple modular redundancy and algorithms for error detection and correction are included to reduce the susceptibility of the implemented SPOT algorithms to space radiations, increasing the system's reliability. A Hardware-in-the-Loop (HIL) setup was developed as well, to verify the performance and robustness of the SPOT algorithms and simulating critical scenarios. The preliminary

experimental results conclude that the hardware SPOT implementation accelerates the execution speed approximately by 100 times compared to a software solution on the Intel CPU. Furthermore, the results between HIL and the numerical simulator show an error under 0.01%.