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COST EFFECTIVE APPROACH FOR A RELIABLE SEE ROBUST DESIGN

Abstract

Nowadays, driven by the market needs to develop products in a short time with a reduced cost, and without impacting the reliability and the quality of the product, different system design techniques that contribute to achieve these objectives are analysed and tested.

Probably the key parameter in space projects is Reliability. This is the reason why, the electronic parts each space equipment is composed of, are designed, manufactured and tested in order to provide high reliability rates withstanding extreme harsh environment. Definitely, high reliability figures are achieved following these practises but use of traditional "High-Reliability" (Hi-Rel) components also presents many drawbacks when it comes to development time, cost and performances. From the technical point of view, the main difference between the traditional Hi-Rel components and the COTS is the Radiation Hardness Assurance (RHA) approach. In the RHA strategy, two main aspects need to be addressed: cumulative effects, and Single Event Effects (SEE).

The proposed on-going development, started by the end of 2021 and with first preliminary results available by mid of this year, is focused on providing a SEE-robust architecture. The sensitivity to destructive and non-destructive SEE of any electronic board will determine its reliability and availability, respectively. The proposed design approach intends to improve these two RAMS disciplines from a pragmatic point of view. The core component is a COTS microcontroller, not fully SEL immune in a Space environment (not reaching ECSS threshold of 60 MeV·cm2/mg) combined with a SEE tolerant architecture based on two microcontrollers running in parallel. On the one hand, current consumption is continuously monitored in the active microcontroller, and in case an event is detected, it is power cycled, and control is transferred to the backup microcontroller. On the other hand, to protect against SEUs, both microcontrollers will run in hot redundancy and a FPGA (SEE-tolerant and reliable device) will act as arbiter, taking in real time the decision of toggling the nominal microcontroller, based on a series of simple rules, achieving a fast transition transparent to system functionality.

This paper is intended to present the results of the analysis and tests performed on the proposed SEE robust design as a cost effective solution for space products.