

IAF ASTRODYNAMICS SYMPOSIUM (C1)
Interactive Presentations - IAF ASTRODYNAMICS SYMPOSIUM (IP)

Author: Mrs. Aswathy Krishnan
Indian Space Research Organization (ISRO), India

Mr. Prasanth Krishna K
Indian Space Research Organization (ISRO), India

Mr. Haridas T R
Indian Space Research Organization (ISRO), India

DESIGN AND IMPLEMENTATION OF AN FPGA BASED CONTROL MOMENT GYRO
CONTROLLER

Abstract

Control Moment Gyro (CMG) is an attitude control actuator used in spacecraft missions demanding high agility with rapid multi-target pointing and tracking capabilities. The implementation of CMG rate and position controllers become significant due to their stringent performance requirements in a spacecraft. The gimbal rate and position control accuracy is significant to minimise the CMG output torque errors.

FPGAs are the best option for implementing multi-rate controllers with asynchronous sampling times as it enables the concurrent execution of various controllers. Besides, they do not pose constraints in the controller implementation with respect to the bit widths of the controller coefficients and parameters. However, this flexibility poses disadvantages in terms of the large design resources utilised and imposes restrictions on the implementation of self-tuning features and programmability of coefficients.

An FPGA was designed integrating all the control algorithms used in the system along with other system functions. The controller structures involve several estimation and compensation algorithms which require a large number of hardware resources including multipliers and adders. In order to extract high performance from the FPGA design while optimising the resources, the system functionality was first decomposed into tasks. The data paths were identified and their interactions were studied. Timing studies were carried out to determine the parallel execution requirements of the multirate loops and other system functionalities. Bit width optimisation of logic modules were carried out to enable their reuse for multiple tasks and thus reduce the hardware resource utilisation. Pipelining was carried out to enable parallel computation of operations across multiple data paths.

Experimental test results of the controller realised in FPGA is presented. The results are compared with that of the stability and controller parameters performance studies done in MATLAB/Simulink. The rate accuracy and stability values achieved are shown to be meeting the system specifications while reducing the hardware utilisation by more than 50