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DESIGN AND IMPLEMENTATION OF RECONFIGURABLE DIGITAL SIGNAL PROCESSING MODULE FOR SATELLITE SYNTHETIC APERTURE RADAR USING FPGA

Abstract

A satellite Synthetic Aperture Radar (SAR) system is an advanced technique for earth observation by gathering images from space in cloudy or dark situations; regardless of the weather or day-night conditions, the SAR sensor can obtain high-resolution target images for different applications. Satellite SAR systems have a macro view for targeted areas, given the wide variability in SAR imaging systems and imaging modes, it is desirable to have a SAR system capable of adjusting its viewing angles, chirp parameters, and frequency bands; the transmitted Chirp signal characteristics determine the SAR image resolution. In order to fully harness the system potential; reconfigurable/adaptive SAR systems are needed, a system that implements an algorithm with the ability to generate a rapid, high resolution, and adjustable chirp signal with minimum hardware complexity, additionally, reduces the memory required for data storage with minimum signal distortion. Such reconfigurability imposes a challenge for SAR system designers. This paper discusses the design and implementation of a digital signal processing module for a Synthetic Aperture Radar (SAR) payload. The module utilizes a Field-Programmable Gate Array (FPGA) to generate a chirp signal, with Digital-to-Analog Converter (DAC) and Analog-to-Digital Converter (ADC) as analog front end, and a Double Data Rate (DDR) memory as storage. The advantages of this implementation are reducing phase error and improving signal quality. This design of the Chirp signal is based on the simplification of the equation representation of the time domain linear FM signals. The details of the design and testing of the module, as well as its performance and potential applications in a SAR satellite project, will be demonstrated and discussed.

Keywords: Spaced-based SAR, chirp generator , FPGA