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DESIGN AND DEVELOPMENT OF A LOCALIZED SMALL SATELLITE COMMUNICATION SUBSYSTEM WITH FPGA-BASED TRANSCEIVER

Abstract

The use of cutting-edge microelectronics enables the development of smaller satellites, like cube satellites (CubeSats), which allows new opportunities in the commercial space market. These small satellites are now being used for telecommunications services in addition to scientific missions, earth observation, and remote sensing. The operation of every satellite, whatever mission it serves, relies on the utilization of various subsystems. Among these is the communications subsystem, consisting of RF transceiver and RF front-end.

Despite the significant investments contributing to satellite technologies, the Philippines continues to depend on the importation of satellite communication equipment, including radio transceivers. This reliance raises concerns regarding cost implications, limitations in customization capabilities, and maintaining control over the technology. To address these challenges and to contribute to the advancement of satellite technology, an attempt to localize the design and development of a radio transceiver that utilizes a Field-Programmable Gate Array (FPGA), as a programmable and flexible device, is proposed. The incorporation of FPGA design allows seamless integration of both the transmitter and receiver functions, as modern FPGAs are known for their reconfigurable nature and high logic capacity.

In this research, the proposed communication subsystem design integrates an FPGA as the transceiver system, interfaced with an RF front-end operating at the ultra-high frequency (UHF) band. The design of the FPGA-based transceiver is a software-defined radio, which will be modeled using Xilinx Vivado. The application will also be responsible for the code generation to be implemented in the FPGA hardware. To align with the size constraints of a CubeSat, the selected FPGA for this application is the Arty A7-35T Board which can be utilized in a 2U CubeSat size at most. On the other hand, the RF front-end will be designed as part of the communication subsystem to effectively assess the functionality of the FPGA-based transceiver.

Furthermore, functional and experimental testing of the localized radio transceiver will be conducted at a local full anechoic chamber (FAC). This controlled environment allows the evaluation of the transceiver's performance without any interference. The measured results e.g., (receiver sensitivity, free-space path loss, antenna gains) will be utilized in the analysis of the radio link budget. This analysis will aid in

assessing the overall performance of the prototype as a laboratory demonstration hardware for small satellite communications application.